1. A circuit for a voltage controlled oscillator having a timing control by a bias circuitry and having a low phase-noise comprising:

a first pair of transistors being of a technology wherein complementary polarity transistors are available, wherein the base of a first transistor of said pair is connected to the drain of a second transistor of said pair and the base of a second transistor of said pair is connected to the drain of said first transistor of said pair of transistors, the sources of said transistors are connected to each other and to a V_{dd} voltage, and the drain of a first transistor of said first pair of transistors is connected to the drain of a first transistor of a second pair of transistors and the drain of a second transistor of said first pair of transistors is connected to the drain of a second transistor of said second pair of transistors;

a power supply supplying said V_{dd} voltage;

a second pair of transistors being of a technology wherein complementary polarity transistors are available, wherein the base of a first transistor of said second pair is connected via a means of a bias circuitry influencing timing control to the drain of a second transistor of said second pair and the base of a second transistor of said pair is connected via said means of a bias circuitry influencing timing control to the drain of said first transistor of said pair, each base is connected to said means of a bias circuitry influencing timing control, the sources of said pair of transistors are connected to each other and to a current source, and each drain of said transistors is connected to a means of a LC-tank;

a means of a bias circuitry influencing timing control;

a current mirror being connected to the sources of said second pair of transistors;

a LC-tank being connected between the drains of said first pair of transistors; and

a differential output comprising two ports being located at both sides of said LC-tank.

2. The circuit of claim **1** wherein said means of a bias circuitry is comprising a combination of capacitors and resistors and a voltage source providing a threshold voltage.

3. The circuit of claim **2** wherein said means of a bias circuitry comprises two capacitors and two resistors and a threshold voltage source, wherein one capacitors is connected between the drain of a first transistor of said second pair of transistors and the base of a second transistor of said second pair and the other capacitor is connected between the drain of a second transistor of said second pair of transistors and the base of a first transistor of said second pair and one of both said resistors is connected on one side to the base of the first transistor of said second pair and the other resistor is connected on one side to the base of the other transistor of the second pair and both resistors are connected to said threshold voltage source on their other sides.

4. The circuit of claim **3** wherein said capacitors are a high quality capacitors.

5. The circuit of claim **4** wherein said high quality capacitors are a metal-insulator-metal (MIM) capacitors.

6. The circuit of claim **3** wherein said resistors are low-noise resistors.

7. The circuit of claim **1** wherein said means of a LC-tank comprises an inductor having a means of providing capacitance connected in parallel.

8. The circuit of claim **7** wherein said means of providing capacitance comprises a variable capacitor (varactor).

9. The circuit of claim **1** wherein said first and second pair of transistors are MOS transistors.

10. The circuit of claim **1** wherein said first and second pair of transistors are BiCMOS transistors.

11. The circuit of claim **1** wherein said first and second pair of transistors are GaAs transistors.

12. The circuit of claim **1** wherein said first and second pair of transistors are bipolar transistors.

13. A circuit for a voltage controlled oscillator having a timing control by a bias circuitry, a reduced power consumption, and a higher frequency stability and a low phase-noise comprising:

a first pair of transistors being of a technology wherein complementary polarity transistors are available, wherein the base of a first transistor of said pair is connected to the drain of a second transistor of said pair and the base of a second transistor of said pair is connected to the drain of said first transistor of said pair of transistors, the sources of said transistors are connected to each other and to a V_{dd} voltage, and the drain of a first transistor of said first pair of transistors is connected to the drain of a first transistor of a second pair of transistors and the drain of a second transistor of said first pair of transistors is connected to the drain of a second transistor of said second pair of transistors;

a power supply supplying said V_{dd} voltage;

a second pair of transistors being of a technology wherein complementary polarity transistors are available, wherein the base of a first transistor of said second pair is connected via a means of a bias circuitry influencing timing control to a means to introduce additional gain and the base of a second transistor of said pair is connected via said means of a bias circuitry influencing timing control to a means to introduce additional gain, each base is connected to said means of a bias circuitry influencing timing control, the sources of said pair of transistors are connected to each other and to a current source, and each drain of said transistors is connected to a means of a LC-tank;

a means of a bias circuitry influencing timing control;

a means to introduce additional gain in the amplification loop;

a current mirror being connected to the sources of said second pair of transistors;

a LC-tank being connected between the drains of said first pair of transistors; and

a differential output comprising two ports being located at both sides of said LC-tank.

14. The circuit of claim **13** wherein said means of a bias circuitry is comprising a combination of capacitors and resistors and a voltage source providing a threshold voltage.

15. The circuit of claim **14** wherein said means of a bias circuitry comprises two capacitors and two resistors and a threshold voltage source, wherein one capacitors is connected between the drain of a first transistor of said second pair of transistors and the base of a second transistor of said second pair and the other capacitor is connected between the drain of a second transistor of said second pair of transistors and the base of a first transistor of said second pair and one of both said resistors is connected on one side to the base of the first transistor of said second pair and the other resistor is connected on one side to the base of the other transistor of the second pair and both resistors are connected to said threshold voltage source on their other sides.

16. The circuit of claim **15** wherein said capacitors are a high quality capacitors.

17. The circuit of claim **16** wherein said high quality capacitor is a metal-insulator-metal (MIM) capacitor.

18. The circuit of claim **14** wherein said resistors are low-noise resistors.

19. The circuit of claim **13** wherein said means of a LC-tank comprises an inductor having a means of providing capacitance parallel connected

20. The circuit of claim **19** wherein said means of providing capacitance comprises a variable capacitor (varactor).

21. The circuit of claim **13** wherein said four pairs of transistors are MOS transistors.

22. The circuit of claim **13** wherein said four pairs of transistors are BiCMOS transistors.

23. The circuit of claim **13** wherein said four pairs of transistors are GaAs transistors.

24. The circuit of claim **13** wherein said four pairs of transistors are bipolar transistors.

25. The circuit of claim **13** wherein said means to introduce additional gain in the amplification loops of the VCO is comprising current amplifiers and related current mirrors.

26. The circuit of claim **25** where in said means to introduce additional gain comprise a third and a fourth additional pairs of transistors of a source-follower type of buffers, wherein the sources of both first transistors of said third and fourth pairs are connected to ground, the bases of both first transistors are part of a current mirror each and the drains of said first transistor are each connected to one of the sources of the second transistors of said third and fourth pairs of transistors and to said means of a bias circuitry, the base of said second transistor of said third pair is connected to the drain of the first transistor of said first pair of transistors and the base of the second transistor of the fourth pair is connected to the drain of the second transistor of said first pair of transistors and the drains of said second transistors of said third and fourth pair are both connected to V_{dd} voltage.

27. A circuit for a voltage controlled oscillator being enabled for very low-power operations having a low phase-noise, a timing control by a bias circuitry, a reduced power consumption, and a higher frequency stability comprising:

a first pair of transistors being of a technology wherein complementary polarity transistors are available, wherein the base of a first transistor of said pair is connected to the drain of a second transistor of said pair and the base of a second transistor of said pair is connected to the drain of said first transistor of said pair of transistors, the sources of said transistors are connected to each other and to a V_{dd} voltage, and the drain of a first transistor of said first pair of transistors is connected to the drain of a first transistor of a second pair of transistors and the

drain of a second transistor of said first pair of transistors is connected to the drain of a second transistor of said second pair of transistors;

a power supply supplying said V_{dd} voltage;

a second pair of transistors being of a technology wherein complementary polarity transistors are available, wherein the base of a first transistor of said second pair is connected via a means of a bias circuitry influencing timing control to a means to introduce additional gain and the base of a second transistor of said pair is connected via said means of a bias circuitry influencing timing control to a means to introduce additional gain, each base is connected to said means of a bias circuitry influencing timing control, the sources of said pair of transistors are connected to each other and to a current source, and each drain of said transistors is connected to a means of a LC-tank;

a means of a bias circuitry influencing timing control;

a means to introduce additional gain in the amplification loop;

a means to actively discharge transistor channels;

a current mirror being connected to the sources of said second pair of transistors;

a LC-tank being connected between the drains of said first pair of transistors; and

a differential output comprising two ports being located at both sides of said LC-tank.

28. The circuit of claim **27** wherein said means of a bias circuitry is comprising a combination of capacitors and resistors and a voltage source providing a threshold voltage.

29. The circuit of claim **28** wherein said means of a bias circuitry comprises two capacitors and two resistors and a threshold voltage source, wherein one capacitors is connected between the drain of a first transistor of said second pair of transistors and the base of a second transistor of said second pair and the other capacitor is connected between the drain of a second transistor of said second pair of transistors and the base of a first transistor of said second pair and one of both said resistors is connected on one side to the base of the first transistor of said second pair and the other resistor is connected on one side to the base of the other transistor of the second pair and both resistors are connected to said threshold voltage source on their other sides.

30. The circuit of claim **29** wherein said capacitors are a high quality capacitors.

31. The circuit of claim **30** wherein said high quality capacitor is a metal-insulator-metal (MIM) capacitor.

32. The circuit of claim **28** wherein said resistors are low-noise resistors.

33. The circuit of claim **27** wherein said means of a LC-tank comprises an inductor having a means of providing capacitance parallel connected

34. The circuit of claim **28** wherein said means of providing capacitance comprises a variable capacitor (varactor).

35. The circuit of claim **27** wherein all transistors are MOS transistors.

36. The circuit of claim **27** wherein all transistors are BiCMOS transistors.

37. The circuit of claim **27** wherein all transistors are GaAs transistors.

38. The circuit of claim **27** wherein all transistors are bipolar transistors.

39. The circuit of claim **27** wherein said means to actively discharge transistor channels is comprising complementary conducting transistors and capacitors.

40. The circuit of claim **39** wherein said means to actively discharge transistor channels is comprising:

a first transistor, wherein the source of said transistor is connected to the drain of the first transistor of said second pair of transistors, the drain of said transistor is connected to the source of said first transistor and the base is connected to a first side of a first capacitor;

a second transistor, wherein the source of said transistor is connected to the drain of the second first transistor of said second pair of transistors, the drain

of said transistor is connected to the source of said second transistor and the base is connected to a first side of a second capacitor;

a first capacitor, wherein its first side is connected to the base of said first transistor and its second side is connected to said means to introduce additional gain in the amplification loop; and

a second capacitor, wherein its first side is connected to the base of said second transistor and its second side is connected to said means to introduce additional gain in the amplification loop.

41. The circuit of claim **40** wherein the second side of said first capacitor is connected to the drain of said first transistor of said third pair of transistors and wherein the second side of said second capacitor is connected to the drain of said first transistor of said fourth pair of transistors.

42. A circuit for a voltage controlled oscillator being enabled for very low current operations having a low phase-noise, a timing control by a bias circuitry, a reduced power consumption, a higher frequency stability, and an enlarged amplitude comprising:

a first pair of transistors being of a technology wherein complementary polarity transistors are available, wherein the base of a first transistor of said pair is connected to the drain of a second transistor of said pair and the base of a second transistor of said pair is connected to the drain of said first transistor of said pair of transistors, the sources of said transistors are connected to each other and to a V_{dd} voltage, and the drain of a first transistor of said first pair of transistors is

connected to the drain of a first transistor of a second pair of transistors and the drain of a second transistor of said first pair of transistors is connected to the drain of a second transistor of said second pair of transistors;

a power supply supplying said V_{dd} voltage;

a second pair of transistors being of a technology wherein complementary polarity transistors are available, wherein the base of a first transistor of said second pair is connected via a means of a bias circuitry influencing timing control to a means to introduce additional gain and the base of a second transistor of said pair is connected via said means of a bias circuitry influencing timing control to a means to introduce additional gain, each base is connected to said means of a bias circuitry influencing timing control, the sources of said pair of transistors are connected to each other and to a current source, and each drain of said transistors is connected to a means of a LC-tank;

a means of a bias circuitry influencing timing control;

a means to introduce additional gain in the amplification loop;

a means to enlarge the amplitude of the oscillations;

a current mirror being connected to the sources of said second pair of transistors;

a LC-tank being connected between the drains of said first pair of transistors; and

a differential output comprising two ports being located at both sides of said LC-tank.

:

43. The circuit of claim **42** wherein said means of a bias circuitry is comprising a combination of capacitors and resistors and a voltage source providing a threshold voltage.

44. The circuit of claim **43** wherein said means of a bias circuitry comprises two capacitors and two resistors and a threshold voltage source, wherein one capacitors is connected between the drain of a first transistor of said second pair of transistors and the base of a second transistor of said second pair and the other capacitor is connected between the drain of a second transistor of said second pair of transistors and the base of a first transistor of said second pair and one of both said resistors is connected on one side to the base of the first transistor of said second pair and the other resistor is connected on one side to the base of the other transistor of the second pair and both resistors are connected to said threshold voltage source on their other sides.wherein said means of a bias circuitry is comprising a combination of capacitors and resistors and a voltage source providing a threshold voltage.

45. The circuit of claim **44** wherein said capacitors are a high quality capacitors.

46. The circuit of claim **45** wherein said high quality capacitor is a metal-insulator-metal (MIM) capacitor.

47. The circuit of claim **43** wherein said resistors are low-noise resistors.

48. The circuit of claim **42** wherein said means of a LC-tank comprises an inductor having a means of providing capacitance parallel connected.

49. The circuit of claim **48** wherein said means of providing capacitance comprises a variable capacitor (varactor).

50. The circuit of claim **42** wherein all transistors are MOS transistors.

51. The circuit of claim **42** wherein all transistors are BiCMOS transistors.

52. The circuit of claim **42** wherein all transistors are GaAs transistors.

53. The circuit of claim **42** wherein all transistors are bipolar transistors.

54. The circuit of claim **42** wherein said means to enlarge the amplitude of the oscillations is comprising an arrangement of resistors and capacitors.

55. The circuit of claim **54** wherein said arrangement of resistors and capacitors is comprising two pairs of a resistor and a capacitor connected in parallel each wherein the first pair of a resistor and a capacitor is connected between the drain of the first transistor of said first pair of transistors and the base of the second transistor of said first pair and the second pair of a resistor and a capacitor is connected between the

drain of the second transistor and the base of the first transistor of said first pair of transistors.

56. A circuit for a voltage controlled oscillator being enabled for low current operation having minimal power consumption, a very low phase-noise, a timing control by a bias circuitry, a higher frequency stability, and an enlarged amplitude comprising:

a first pair of transistors being of a technology wherein complementary polarity transistors are available, wherein the base of a first transistor of said pair is connected to the drain of a second transistor of said pair and the base of a second transistor of said pair is connected to the drain of said first transistor of said pair of transistors, the sources of said transistors are connected to each other and to a V_{dd} voltage, and the drain of a first transistor of said first pair of transistors is connected to the drain of a first transistor of a second pair of transistors and the drain of a second transistor of said first pair of transistors is connected to the drain of a second transistor of said second pair of transistors;

a power supply supplying said V_{dd} voltage;

a second pair of transistors being of a technology wherein complementary polarity transistors are available, wherein the base of a first transistor of said second pair is connected via a means of a bias circuitry influencing timing control to a means to introduce additional gain and the base of a second transistor of said pair is connected via said means of a bias circuitry influencing timing control to a means to introduce additional gain, each base is connected to said means of a bias circuitry influencing timing control, the sources of said pair of transistors are

connected to each other and to a current source, and each drain of said transistors is connected to a means of a LC-tank;

a means of a bias circuitry influencing timing control;

a means to run buffer-inverters in class C mode;

a means to enlarge the amplitude of the oscillations;

a current mirror being connected to the sources of said second pair of transistors;

a LC-tank being connected between the drains of said first pair of transistors; and

a differential output comprising two ports being located at both sides of said LC-tank.

57. The circuit of claim **56** wherein said means of a bias circuitry is comprising a combination of capacitors and resistors and a voltage source providing a threshold voltage.

58. The circuit of claim **57** wherein said means of a bias circuitry comprises two capacitors and two resistors and a threshold voltage source, wherein one capacitors is connected between said means to run buffer-inverters in class C mode and the base of a second transistor of said second pair and the other capacitor is connected between said means to run buffer-inverters in class C mode and the base of a first transistor of said second pair and one of both said resistors is connected on one side to the base of the first transistor of said second pair and the other resistor is connected on one side to

the base of the other transistor of the second pair and both resistors are connected to said threshold voltage source on their other sides.wherein said means of a bias circuitry is comprising a combination of capacitors and resistors and a voltage source providing a threshold voltage.

59. The circuit of claim **58** wherein said capacitors are a high quality capacitors.

60. The circuit of claim **59** wherein said high quality capacitor is a metal-insulator-metal (MIM) capacitor.

61. The circuit of claim **57** wherein said resistors are low-noise resistors.

62. The circuit of claim **42** wherein said means of a LC-tank comprises an inductor having a means of providing capacitance parallel connected.

63. The circuit of claim **62** wherein said means of providing capacitance comprises a variable capacitor (varactor).

64. The circuit of claim **56** wherein all transistors are MOS transistors.

65. The circuit of claim **56** wherein all transistors are BiCMOS transistors.

66. The circuit of claim **56** wherein all transistors are GaAs transistors.

67. The circuit of claim **56** wherein all transistors are bipolar transistors.

68. The circuit of claim **56** wherein said means to enlarge the amplitude of the oscillations is comprising an arrangement of resistors and capacitors.

69. The circuit of claim **68** wherein said arrangement of resistors and capacitors is comprising two pairs of a resistor and a capacitor connected in parallel each wherein the first pair of a resistor and a capacitor is connected between the drain of the first transistor of said first pair of transistors and the base of the second transistor of said first pair and the second pair of a resistor and a capacitor is connected between the drain of the second transistor and the base of the first transistor of said first pair of transistors.

70. The circuit of claim **56** wherein said means to run buffer-inverters in class C mode is comprising transistors amplifying and inverting the signals while other transistors are providing biasing currents.

71. The circuit of claim **70** wherein said means to run buffer inverters in class C mode comprise two lines of concatenated transistors, wherein the first line of concatenated transistors comprises:

a first transistor, wherein the gate and the drain is connected to V_{dd} voltage and the source is connected to the source of a second transistor;

a second transistor, wherein the gate is connected to a first leg of said LC-tank and to the base of a third transistor and the drain is connected to the drain of a third transistor and to said means of bias circuitry;

a third transistor, wherein the source is connected to the drain and to the gate of a fourth transistor; and

a fourth transistor, wherein the source is connected to ground;

and wherein the second line of concatenated transistors comprises:

a first transistor, wherein the gate and the drain is connected to V_{dd} voltage and the source is connected to the source of a second transistor;

a second transistor, wherein the gate is connected to a second leg of said LC-tank and to the base of a third transistor and the drain is connected to the drain of a third transistor and to said means of bias circuitry;

a third transistor, wherein the source is connected to the drain and to the gate of a fourth transistor; and

a fourth transistor, wherein the source is connected to ground.

72. The circuit of claim **71** wherein the connection between the drain of the second transistor of said first line of transistors to said means of bias circuitry is performed via the capacitor being connected to the gate of the first transistor of said second pair of transistors and the connection between the drain of the second transistor of said second line of transistors to said means of bias circuitry is performed via the capacitor being connected to the gate of the second transistor of said second pair of transistors.